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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/956,994	09/21/2001	Mutsumi Kimura	110423	2948

25944 7590 08/24/2006

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EXAMINER	
LEWIS, DAVID LEE	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

BV

Office Action Summary	Application No.	Applicant(s)	
	09/956,994	KIMURA, MUTSUMI	
	Examiner	Art Unit	
	David L. Lewis	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1, and 3-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (5349366) in view of Yamazaki (6545656).**

As in claim 1, 9, 10, 11, 12, 15, and 16, Yamazaki (366) et al. teaches of a driving method for an electro-optical device which includes, corresponding to an intersection of a scanning line, **figure 1A item Vg**,

and a data line, **figure 1A item Vd**,

a power line, **figure 1A item VLC**,

an electro optical element, **figure 1A item LC**,

a driving transistor that controls a current flowing through the electro-optical element, **figure 1A item Tr2,**

and a switching transistor that controls the driving transistor, **figure 1A item Tr1,**

a drive circuit, **column 17 lines 30-40,** implicit to figure 6A and 8A, having **scan line drivers** to produce signal Vg controlling a switching transistor to turn off and on (conducting and non-conducting) and a **data line driver** to produce signal Vd to control the driving transistor to turn off and on (conducting and non-conducting),

the driving method comprising: a setting step of supplying a first on-signal to switching transistor via the scanning line, **figure 1B item Vg (t0),**

and of supplying a set signal to select a conducting state or non-conducting state of the driving transistor to the driving transistor via the date line and the switching transistor in accordance with a period for which the first on-signal is supplied, **figure 1B item Vd (t0);**

the driving transistor controlling the supply of power between the power line whose potential is constant and the electro optical element, **figure 1B item V1 (t0 to t2);**

and a resetting step of supplying a second on-signal to the switching transistor via the scanning line, **figure 1B item Vg (t2)**, column 11 lines 3-10

and of supplying a reset signal to select the non-conducting state of the driving transistor to the driving transistor via the data line and the switching transistor in accordance with a period for which the second on-signal is supplied, **figure 1B item Vd (t2)**, column 11 lines 3-10.

wherein the period for which the first on-signal is supplied coincides with a period for which the set signal is supplied**, figure items Vg and Vd, t=t0**.

a horizontal scanning period that includes a first horizontal scanning period, to perform the setting step, **figure 1(B) times t=to to t=t2**,

and a second horizontal scanning period to perform the resetting step, **figure 1(B) times t=t2 to t=tz**, where tz is the repreated period of t2, as repeated in figures 3(B) and 6(A).

Wherein the pixel is turned on in the first frame period (t0-t1), the pixel maintains the on state in the second frame period (t1-t2) and is turned off in the third frame period (t2+). Said turn off the third frame period is equivalent to a reset during

time t2. Further wherein the frame periods are equivalent to the horizontal scanning periods given signal Vg corresponds to the scanning signal.

However Yamazaki (366) fails to specifically teach of sub horizontal scanning periods or vertical scanning periods.

Yamazaki (656) teaches of sub frame periods which are equivalent to the sub horizontal scanning periods, as shown in **figures 2 and 3**, wherein a set D1 and reset R signals are performed in a first and second sub frame periods which are equivalent to the sub horizontal scanning periods, which occur within a main frame period.

As applied to claim 11 wherein a period of supplying the signal to reset the driving transistor via the data line with a vertical scanning period being substantially constant is shown by Yamazaki (656), figures 2 and 3, wherein said set and reset signals are shown to be provided with the period of one frame, which is equivalent to the period within a vertical scanning period which occurs every frame as known in the art.

As in claim 12, Yamazaki et al. (366) teaches of the number of signal to perform the setting and the signal to perform the resetting being substantially the same, figure 1(B) items Vg @ t0 and Vg @ t2.

As in claim 15, Yamazaki et al. (366) teaches of a plurality of set and reset ooperations being performed in one frame having mutually different time lengths, figure 1(B) signal Vg, and figure 6(A) signal Vg, wherein Yamazaki (656) expands on the idea of said plurality of set and reset, figures 2, 3, 26, and 27.

Therefore while Yamazaki (366) fails to teach of said sub horizontal scanning period, **said feature would have been obvious to the skilled artisan at the time of the invention given** Yamazaki (656) suggests a device as taught by Yamazaki (366) can have multiple sub frames to perform set and reset function of the display, as taught by both Yamazaki (336 and 656), as found in claims 1, 9, 10, 11, 12, 15, and 16. The motivation to combine Yamazaki (336 and 656) is found in the fact that both teach of like matrix displays having set and reset functions within multiple frames. Said set and reset functions are useful for providing a quality display as known in the art. Further, said feature as taught by Yamazaki (656) including supplying the reset signal within a vertical scanning period being substantially constant is also taught suggests by Yamazaki, wherein it would have been obvious to the skilled artisan at the time of the invention to provide said feature because Yamazaki teaches of providing set and reset signals within one main frame period which implies a vertical scanning period as known in the art and applied to claim 11

As in claims 3, Yamazaki et al. teaches of, further including performing the setting step in a first horizontal scanning period, **figure 1(b) signal Vg @ t0**, and performing the resetting step in a second horizontal scanning period, **figure 1(b) singal Vg @ t2**.

As in claim 4, Yamazaki et al. teaches of further including obtaining a gray-scale by performing a plurality of set-reset operations, **figure 1(B)**, each set-reset operation including the setting step and the resetting step, **figure 1(B)** as applied to claim 1 and further, **column 16 lines 35-67, figure 6A**, wherein said gradation is performed according to said method of claim 1 having a set and reset between t0 to t2+

As in claim 5, Yamazaki et al. teaches of further including providing a time interval between the setting step and the resetting step that is different for each of the plurality of set reset operations, figure 6 A signal Vg, wherein the resetting is shown by the switching of signal V1, column 21 lines 63-68.

As in claim 6, Yamazaki et al. teach of the time interval between the setting step and reseting step to be completely different from each other, figure 1(B) and 6(A) signal V1, and column 21 lines 63-68, whererin pixels can be addressed at periods long than the period of alternating potential V2, Yamazaki fails to teach of said ratio of time intervals for the purallity of set-reset operations being set to

1:2n, baseond on the minimum time interval. Yamazaki (656) suggests the setting and resetting steps be at different regular intervals based on a minimum value as shown in the alternative differences provided by figures 2, 3, 26, and 27. It would have been an obvious design choice to provide for said ratio because Yamazaki suggests a ratio based on regular intervals in a system as taught by Yamazaki, as found claim 6.

As in claim 7, Yamazaki et al. teaches of, further including providing the set signal to be a signal for setting the conducting state for the driving transistor rather than the signal for selecting the conducting state or the non-conducting state of the driving transistor, **figure 1B item Vg (t1-t2)**.

As in claim 8, 13, and 14, Yamazaki et al. teaches of, further including driving the electro-optical element including an organic electroluminescence element, figure 1A item LC.

Response to Arguments

2. Applicant's arguments filed 7/31/2006 with respect to claims 1 and 3-16 have been considered but are moot in view of the new grounds of rejection. See the rejection over Yamazaki et al in view of Yamazaki. Applicant argues Yamazaki (656) fails to overcome the deficiencies of Yamazaki (366), the Examiner

disagrees because Yamazaki (656) teaches of sub frames which are equivalent to said sub horizontal scanning periods, and include a verticlal period as known in the art.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on MT and THF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the

examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.

5. Please note that all future correspondences directed to David L. Lewis must be sent to Art Unit 2629.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: David L. Lewis

August 21, 2006